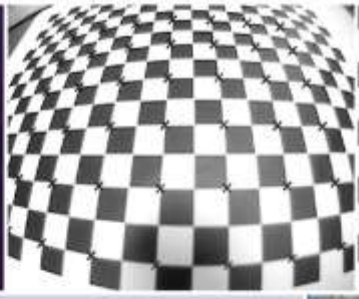
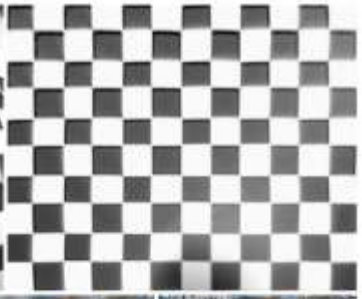


ASIC, EPLD and IP for Camera Systems



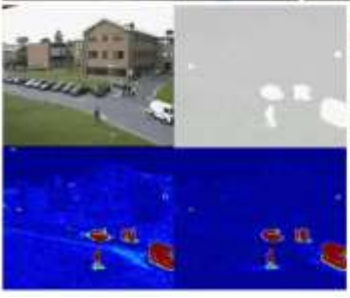
eyenix

www.eyenix.com

The great eyes of the world !!

Founded in 2002, Eyenix provides total image solutions for all kinds of camera systems, security, camcorder, mobile camera and IR camera based on algorithm development, image analysis, and EPLD design. We mainly focus on development of SoC digital camera processors for image sensors, and research on IP solutions such as image restoration, pattern recognition, image stabilization, motion detection and image scaling.

Intelligent Vision Systems



EN293

Multiple Object Detector

Description

Embedded MOD technology detects, tracks and also recognizes multiple moving objects while ignoring trivial movements generated by light changes, moving cloud shadows, swaying branches, rain and snow.

Adaptive background model and probability based foreground motion detection algorithm dramatically decrease false alarm rate less than 1% at 99% detection accuracy.

Appearance model based tracking and recognition modules make possible to continuously keep the track of moving objects and to classify them into three categories, human, car and trivial objects.

Two simultaneously processing blocks consisting of EPLD and DSP parts, detect max. 255 objects of min. 3x8 pixel size at a great distance, max. 4km, at 30 frames per second, as well as track 12 moving objects. The MOD unit can operate on all types of stationary cameras, B/W, color, thermal, and infrared, and on all kinds of applications such as indoor, outdoor, and military uses.

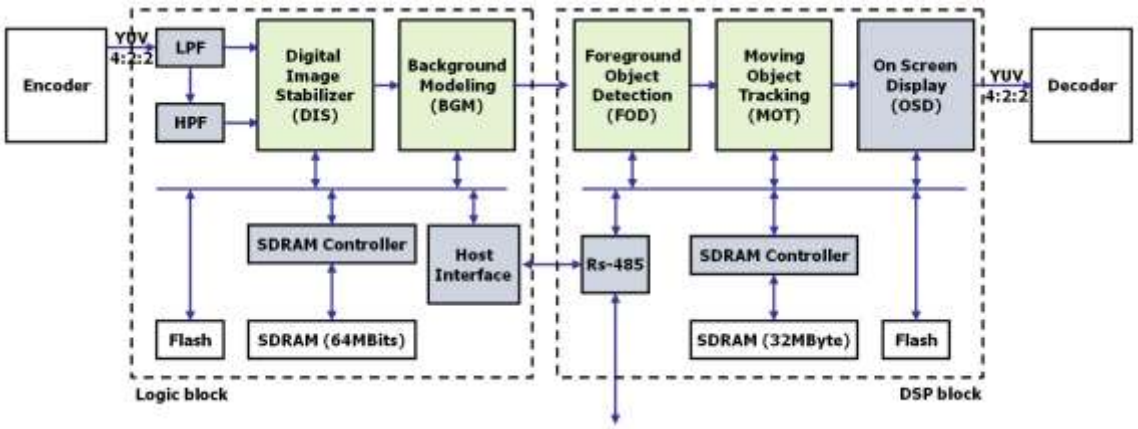
Features

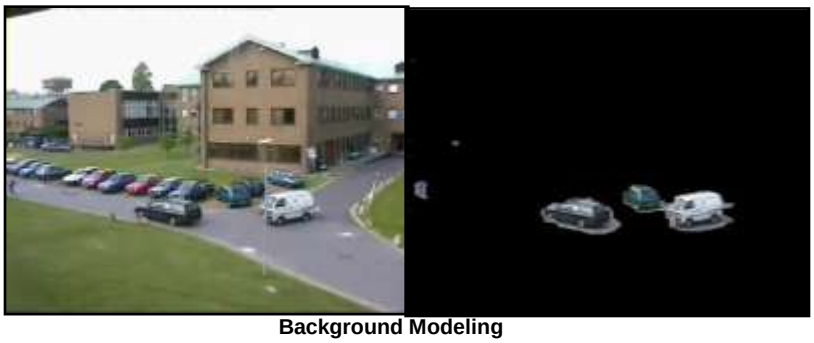
- Adaptive background
- Automatic scene change detection
- Probability based motion detection
- Appearance model based motion tracking
- Multiple object detection and tracking
- Motion trajectory display
- Object recognition
  - human, vehicle, or nothing

Specification

Input Channels	1 – 2 Ch	
Video Data Input	ITU-R656 4:2:2 8 bits / ITU-R601	
Video Data Output	ITU-R656 4:2:2 8 bits / ITU-R601	
Video Format	NTSC / PAL	
Processor	ALTERA - EP2S60	TI - 320C6416
Processing Speed	30 fps	
Operating Freq.	27MHz	1GHz
Filters/Algorithm	MAIIR / BGM NR / CCL DIS	Prob. based FOD AM based MOT Traj. Management Obj. Recognition
Detection Size	Min. 3x8 pixels	
Detection Range	Max. 4 Km	
Detection Count	Max. 255 Objects	Max. 12 Tracks
False Alarms	Less 1% @ 99%	
Code	Verilog RTL coding	C/C++
Operating Temperature	-20°C ~ +85°C	
Power	5V	

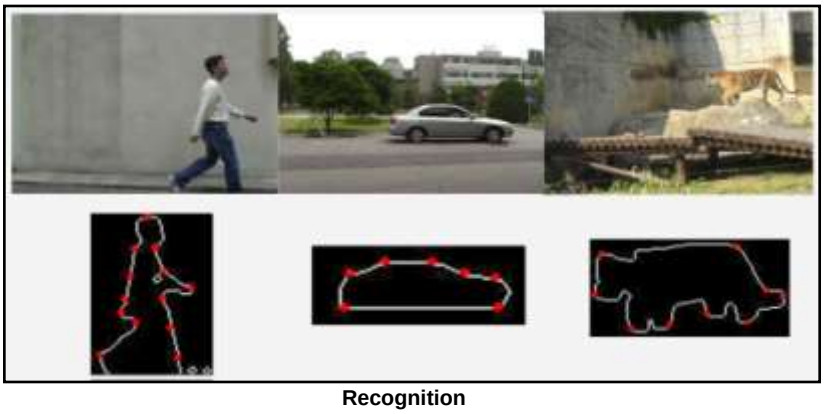
Block Diagram





Background Modeling

Parking Violation Detection



Recognition

Tracking for Military Use

Tracking for Nonmilitary Application

FaceDet

Face Area Detector

Description

Eyenix's new Face Area Detection Technology automatically detects human face candidates in the picture and simultaneously analysises these areas.

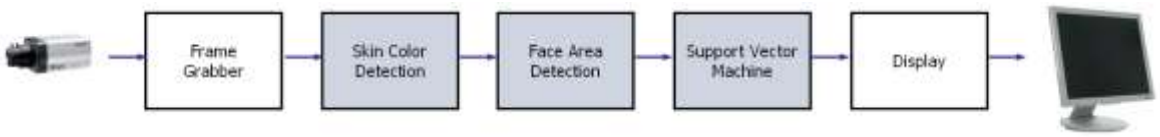
Using this information, camera system is able to focus on the face areas, and camera can intelligently execute the best possible white balance, focus, exposure or flash levels for shaper, more natural and beautiful photos in the view of the human face.

Since the system can evaluate a number of human faces at once, it will provide the best focus information to the user.

Specification

Processor	DSP or FPGA
Processing Speed	over 30 fps
Operating Freq.	27MHz
Algorithm	Skin Color Detection Face Area Detection Support Vector Machine
Detection Size	Min. 20x23 pixels
Detection Count	TBD

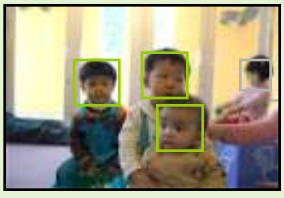
Block Diagram



Example of Multiple Face Area Detection

Auto Focus Application

Auto Exposure Application



Auto White Balance Application

Fixed Zone

Face Adaptive Zone

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A-DNR

Advanced Digital Noise Reducer
Based on Spatiotemporal Template matching

Description

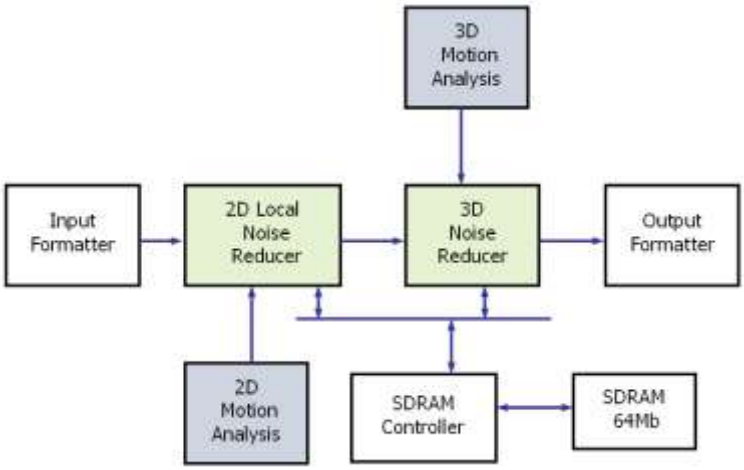
The A-DNR is motion-compensated temporal noise reduction filter leads to effective noise reduction for motion video without blurring.

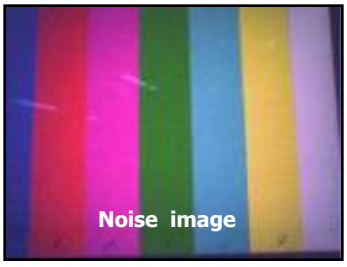
The algorithms are based on accurately measurement of the local motion in a given video sequence, and local time averaging based on the degree and direction of motion. This spatiotemporal de-noising can reduce flickers in intra-frame as well as random noise in time.

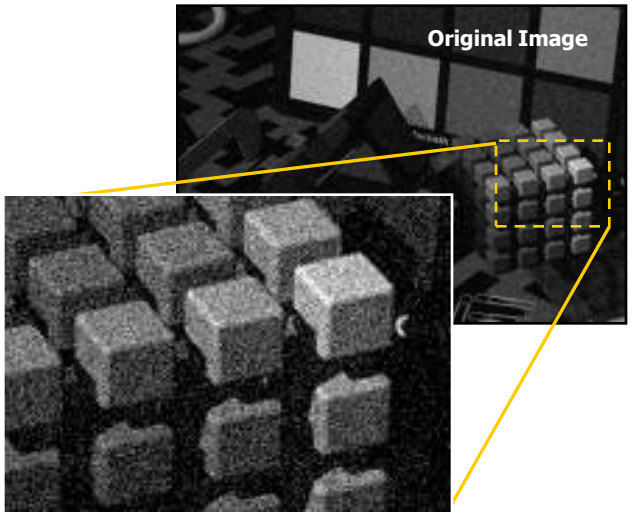
Features

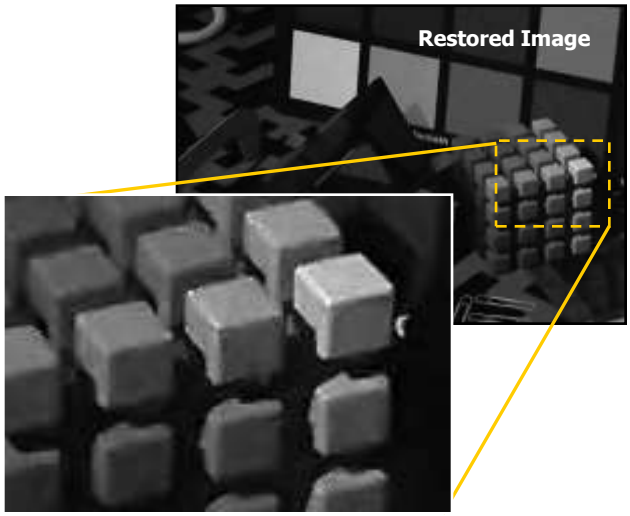
Motion aligned 3D noise reduction
Random noise reduction
Flicker reduction
Lower artifacts (Lag effect, Local noise…)

Block Diagram









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EN170

Digital Image Stabilizer for NTSC/PAL Video system

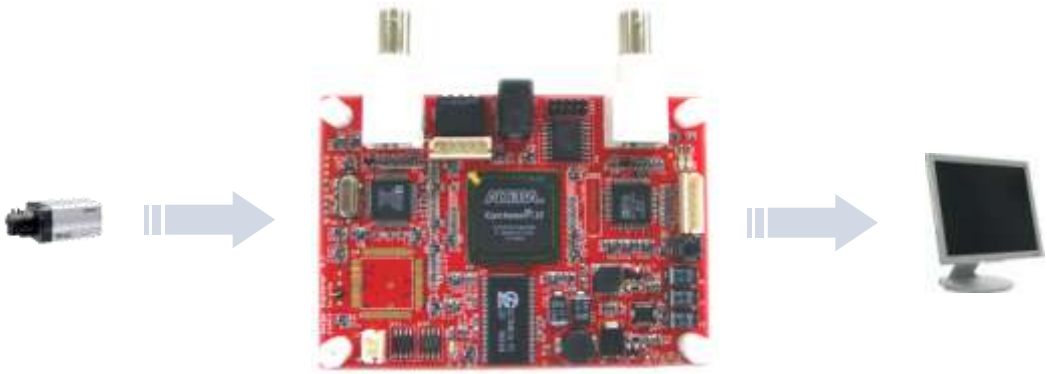
Description

Digital Image Stabilizer, DIS, corrects video shaking which occurs in a camera. DIS detects the amount of camera movement caused by handshaking or outer vibration of the camera, and compensates its shifted image stably. DIS module provides the best performance in drift correction with sub-pixel accuracy at all kinds of scenes.
The clear image can be achieved under the outdoor unstable condition caused by large optical zoom, more than x30, as applying to video camera systems, security camera or camcorder.

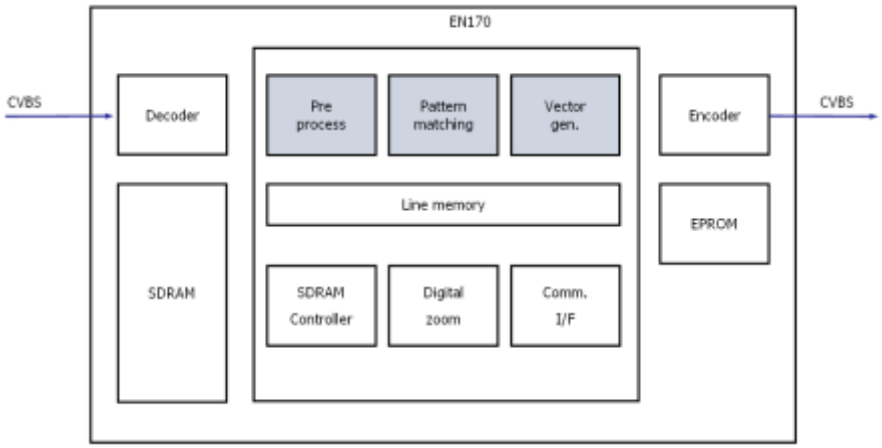
- Correcting unsteady images in real time
- Correcting pre-recorded media in addition to live video
- Setting motion detection area for detecting motions in video
- Provides sub-pixel level correction precision
- Correction accuracy measurable in sub-pixels is
- Simple design-works just by connecting video cable without special connections
- Compact, DC operation

Specification

H/W	Verilog RTL coding
Algorithm	Pattern SAD
Motion vector range	+/- 32 pixel per field
Compensation margin	Max +/- 128 pixels (30% per total)
Detection area	Flexible
Motion accuracy	1/64 pixel
Extended mode	Extended DIS without Dzoom
Digital zoom mode	apply (max x256)
Frame Delay	1 frames
Power	DC 5V
Max Current	0.3A
Main CLK	27MHz
OP Temperature	-20℃ ~ 70℃
I/O video	CVBS (75ohm) NTSC / PAL
SDRAM	64Mbit



Block Diagram



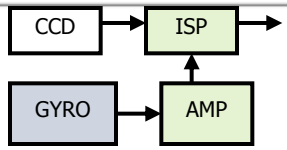
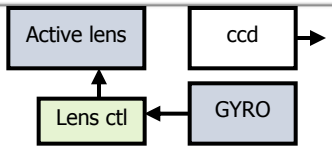
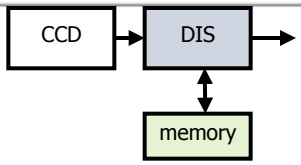
Motion blurred image

Compensated image

Motion blurred image

Compensated image

System (EIS, OIS) Comparison

	EIS (Electrical Image Stabilizer)	OIS (Optical Image Stabilizer)	DIS (Digital Image Stabilizer)
functions	+ Gyro Sensor (x/y axis) + Skip line controllable Timing generator	+ Active Prism + Mechanical actuator (lens)	+ Image processing + Memory buffer (SDRAM)
block diagram			
algorithm	CCD Read Point Control by detecting gyro sensor motion as camera's unstable movement.	Camera flexible lens axis control by detecting gyro sensor motion as camera's unstable movement.	Motion of image series detected by image processing and compensated the unstable motion by memory readout control.
cost	Normal	High (mechanical H/W platform)	Low (ASIC)
feature	Not depending image quality as like dark image.	High image quality. Normally digital camera system applied.	High responsibility of motion correction. Small system packaging. Easy SoC with special effects.
weak point	Low accuracy in high zoom magnification. Size limitation. Temperature variance.	High cost	Low correction performance in noisy and dark image.
Problems	High accurate MEMS technology	Small Active lens	ISP design

DRC

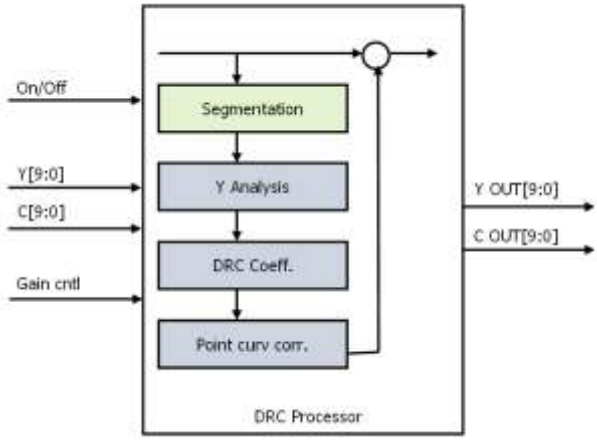
Dynamic range compressor (IP)

Description

Dynamic range compression is necessary because imaging devices has narrow dynamic range. Conventional methods, such as Gamma Correction or Histogram Equalization, are normally lost their contents information in limit area, and then picture quality of bright/dark area can be degraded.

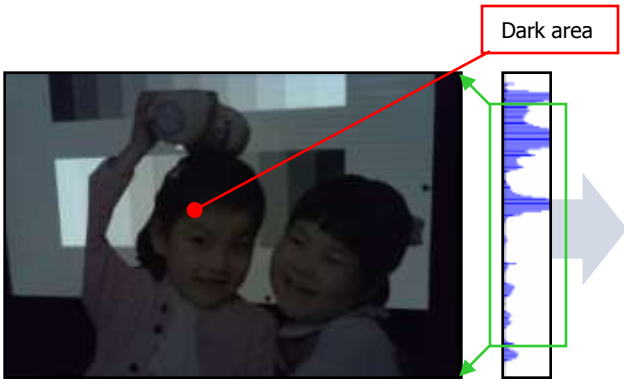
Eyenix's DRC processing is based on the human visual system. The DRC automatically calculates a different curve transformation for each pixel in image, based on an analysis of the image segmentation. Processed result image is capable of drastic dynamic range compression, while preserving fine details and avoiding common artifacts, gradient reversals or loss of local contrast.

Block Diagram

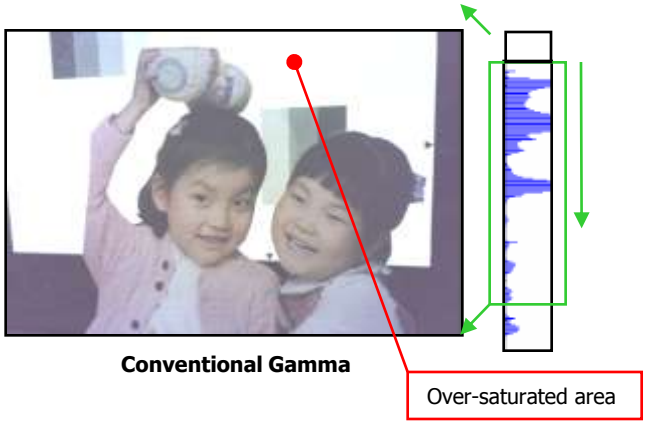


Features

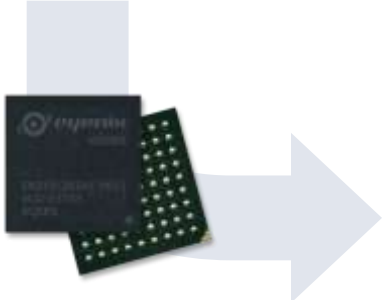
High Quality dynamic range compression
Histogram based contrast enhancement
Adaptive Gamma control
Lower artifacts FPGA Implementation
Hardwired IP CORE
Not required Special DSP or CPU



Back-lighted Original image



Conventional Gamma



Eyenix DRC

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HRDiZ

High Resolution Digital Zoom Based on Multiple Image

Description

The HRDiz is a high resolution digital zoom processor based on multiple image.

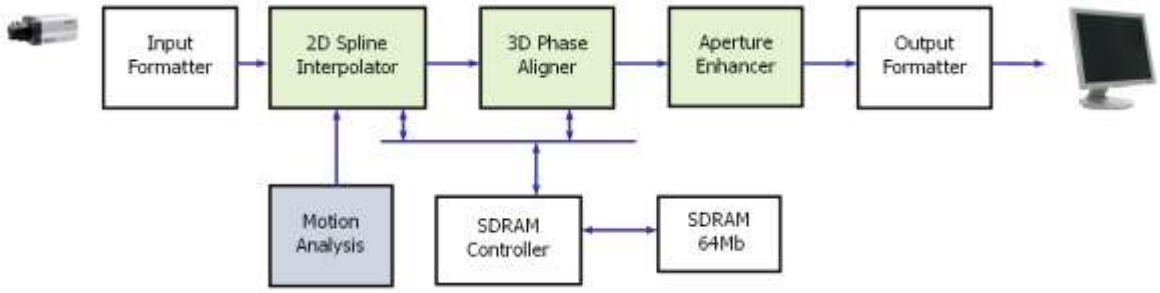
Generally, A image changes more magnifying digitally, then make less sharpness and vivid. The HRDiz can produce sharp and clear zoomed image without critical loss of image resolution. The HRDiZ consists of 3D motion-compensated image mixer, 2D adaptive Spline interpolator and Aperture enhancement algorithms simultaneously.

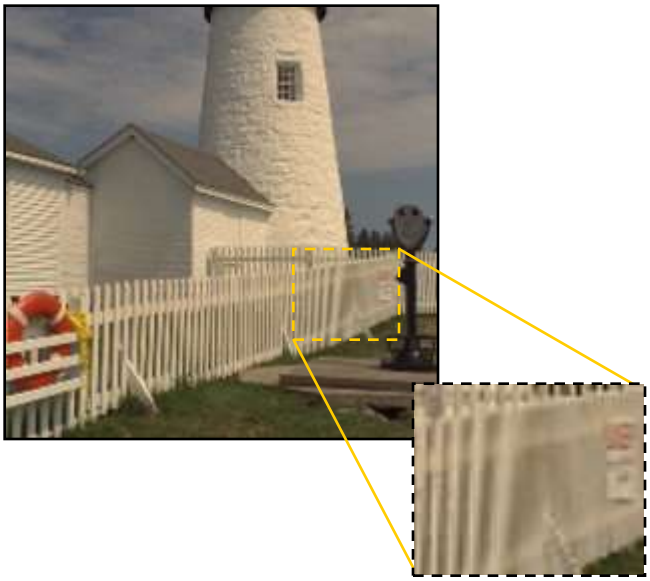
The algorithms are based on accurately measurement of the local motion in a given video sequence, and local time averaging based on the degree and direction of motion.

Specification

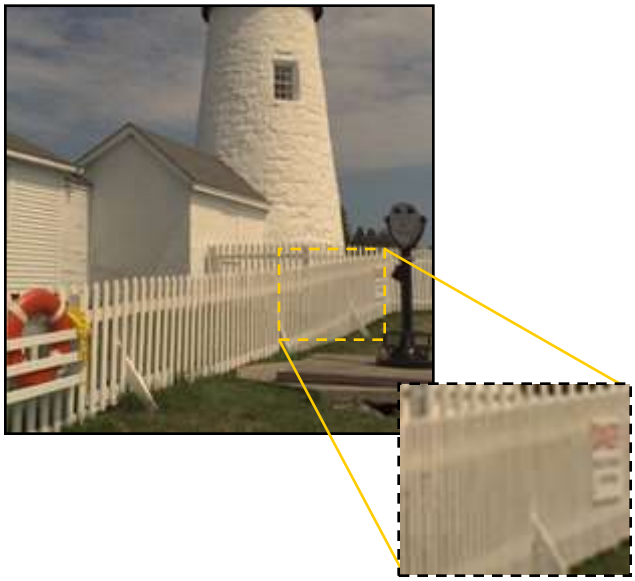
H/W	Input pixels	~ 1.3M pixels 30P/60i
	Imager	CCD / Global Shutter CIS
	Internal SRAM	7H lines (8x8 mask window)
	Control Parameter	64bit Registers (TBD)
	I/O Format	Bayer RGB / YUV
Algorithm	3D Motion Alignment, Spline Digital Zoom	
Evaluation	Altera FPGA @30MHz Clock	

Block Diagram





Bi-Linear Zoom



High Resolution Digital Zoom

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ISP for Car Vision

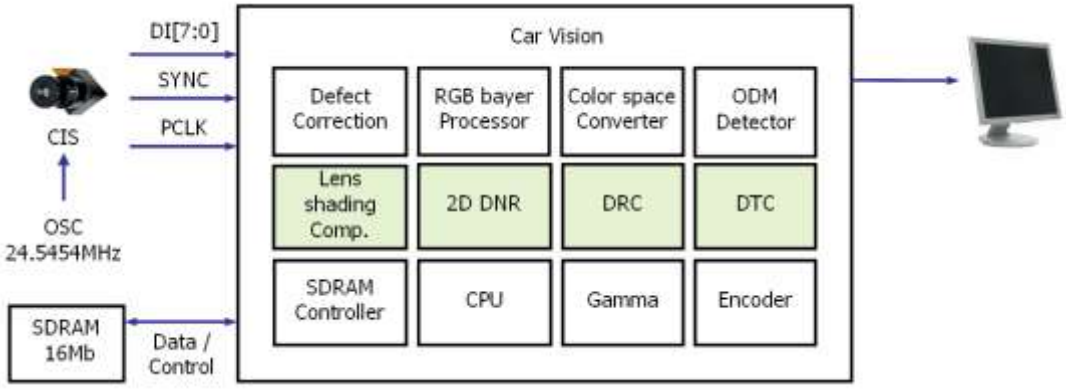
Image Signal Processor
Built in Distortion and Top-View correction

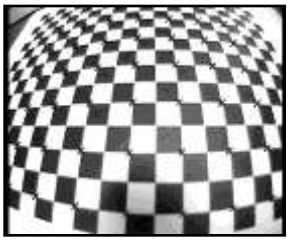
Features

- Horizontal/Vertical Lens Distortion Correction (Digital Zoom)
- Lens Shading Compensation
- 2D-DNR (Dynamic Noise Reducer)
- AE/AWB Detector
- 256 Defect Correction
- Top view mode
- Composite video output (Embedded Encoder & DAC)
- Embedded CPU

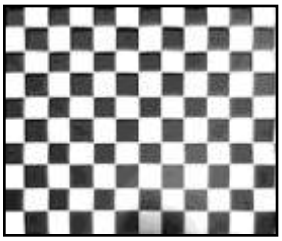
Specification

Resolution	640x480 VGA Cmos Sensor
Operating Freq.	24.5454Mhz (int. 49.0908MHz)
Video Data Input	10 bit parralel input
Video Data output	Encoder output
Video Format	NTSC / PAL
Lens shading comp.	Yes
Digital noise reducer	Yes
DRC	Yes
Controllable Gamma	Yes
DTC	Yes
Power Down mode	Yes
External Memory	SDRAM 16Mb
CPU	32bit EISC
Operating Temperature	-40°C ~ +120°C
Supply Voltage	Core 1.2V, I/O 3.3V





Original Image



Corrected Image

Original Image

Corrected Image

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EN910

Stereo 3D Depth Detector SoC

Description

Eyenix's EN910 is a stereo matching processor that is designed for artificial vision systems of mobile robots. This chip can support VGA to SXGA inputs from Bayer RGB CMOS sensors and output at YUV video format.

The algorithms is based on the sum of absolute difference (SAD) of correlation-based methods to provide disparity map, the disparities of all the image points. Disparity is computed up to 64 pixels at 30 frames per second at Max. 30 MHz. And also the output is precisely interpolated at 1/32 pixel resolution. Using camera geometric information, the disparity map can be converted into three dimensional map which can be used for inferring the structural information, such as the distance from the camera, of a 3D scene.

This chip can be used for mobile robots, automatic vehicle navigation, and intelligent security systems.

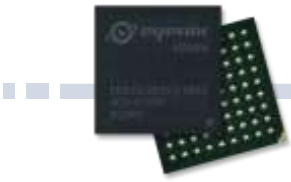
Specification

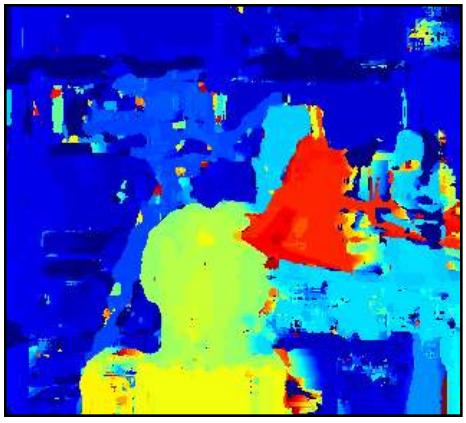
H/W	Imager	VGA ~ SXGA (1.3M)
	Video Input	Bayer RGB CMOS Sensor
	Video Output	YUV / RGB
	Interface	Parallel / LVDS
	I/O Format	YUV / RGB
	Frame rate	30 FPS
	Clock	Max. 30 MHz
Algorithm	Segmentation based adaptive SAD	
Stereo Matching	Template Size	3x3 ~ 11x11 user define
	Disparity Max	64 (TBD)
	Subpixel resolution	1/32

Stereo Vision System

Left image

Right image





Disparity map

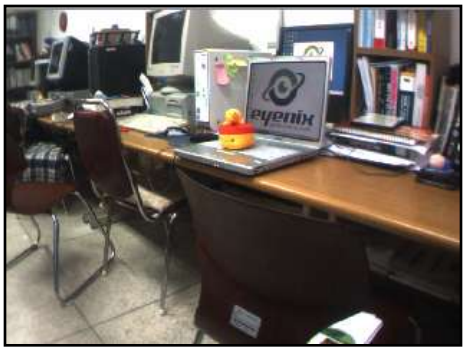
Evalution Board

FEATURES

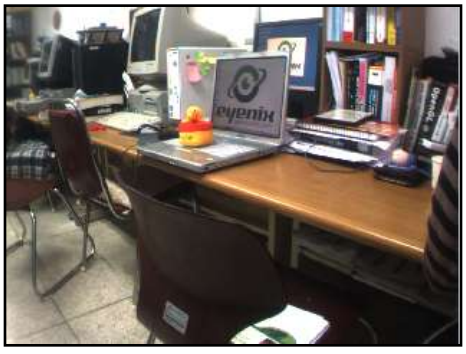
. Capable of disparity detection in real time
. Correction accuracy measurable in sub-pixels
. Simple design-works just by connecting video cable without special connections
. Compact, DC operation

SPECIFICATION

H/W	Imager	Dual Head CMOS Sensor
	Processor	ALTERA – EP2S60 ALTERA – EP2C50
	Video Output	DVI, PC Monitor
	Interface	USB, RS232, Serial
	I/O Format	Bayer RGB / YUV



Left image



Right image

3D Images

eyenix
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