EN675
Brief Datasheet

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Apr. 13, 2021

Document Description

This is the document to describe the Brief Datasheet which is applied to EN675.

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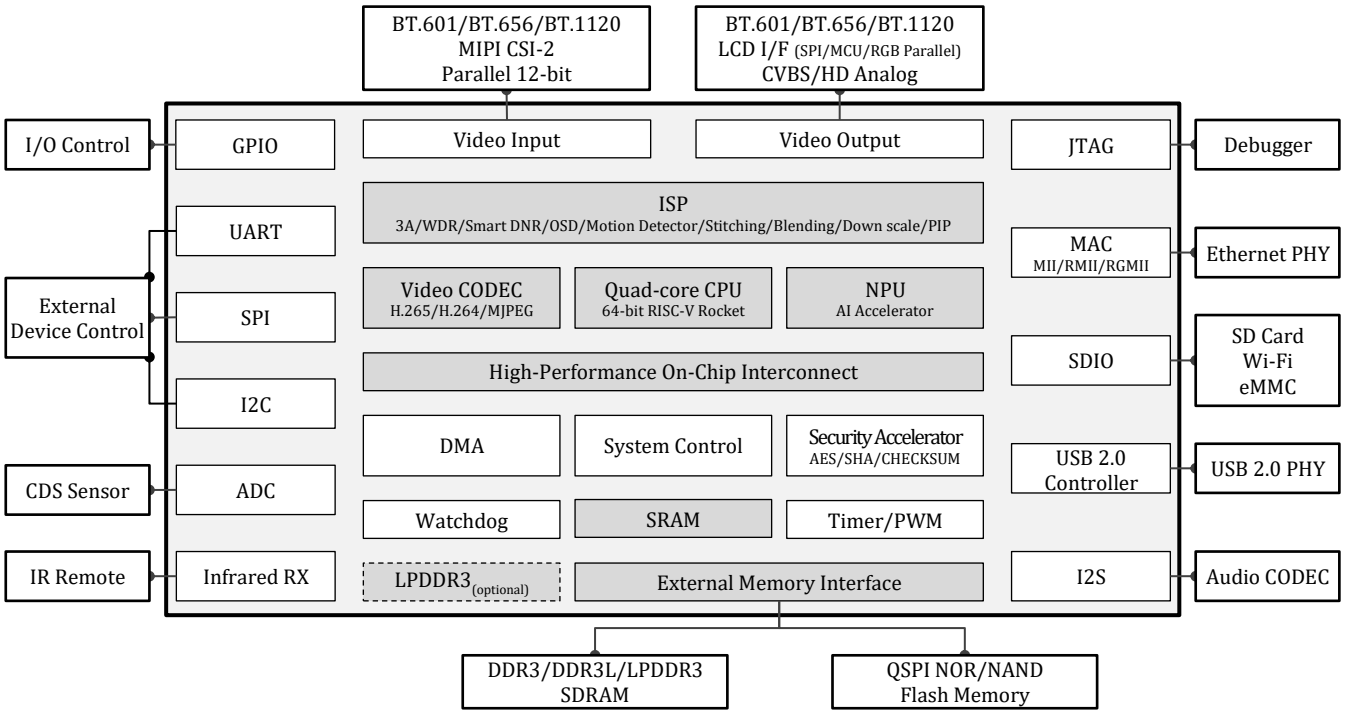
1. General Description

The EN675 SoC provides high-performance consumer product line and IP camera solutions. The ISP inside supports image enhancement and noise reduction functions such as 3A (AE, AF, AWB) and ADNR. It also supports a various type of analog and digital image sensor interfaces to work and control seamlessly in image processing path. A multi-channel digital input from outside is capable, and supports PIP, Image stitching and Image blending functions which can change channels flexible. Also, it supports LCD Interface (Parallel, SPI), CVBS and digital outputs. The EN675 adopts H.265+, H.264+, JPEG, and MJPEG to enable encoding and decoding with multiple resolutions. This chip provides wired/wireless network, SD card, USB storage functions through USB 2.0 MAC, Ethernet MAC (10/100/1000Mbps), and SDIO. The 64-bit RISC-V based quad-core CPU is embedded in SoC to leverage performance and power consumption. The debugger and compile environment are provided for developer's convenience. Linux, FreeRTOS, and BareMetal are portable across platform and to simultaneously run multiple operating systems.

2. Block Diagram



3. Features

Processor Core
- 64bit RISC-V Quad core up to 594MHz
  - 16KB I-cache, 16KB D-cache
- Integrated double-precision FPU
- JTAG (33MHz hi-speed JTAG debug)
- 256KB on-chip SRAM

Video Codec
- H.264/265 Encoder
  - Real-time hard-wired H.264/265 encoding
  - 5M 30fps + HD 30fps + VGA 30fps
  - 4K 30fps + VGA 30fps
- H.264/265 Decoder
  - Real-time hard-wired H.264/265 decoding
  - 4K 30fps
- JPEG Encoder/Decoder
  - Up to 4K 30fps
- H.265 + H.264 + MJPEG triple-streaming
- CBR/VBR control

Image Processing
- RGB interpolation
- Multi-exposure WDR (line-interleaved-sensors) with local tone mapping
- 3 Auto controller (AE, AF, AWB)
- 2D/3D adaptive digital noise reducer
- Adaptive contrast enhancement
- Auto defect detection and correction
- Edge enhancement
- Gamma correction
- HUE controller
- Pseudo color suppression
- Highlight masking
- Moving object detection
- OSD (Box, Font)
- 4 channel down scaler
- Digital zoom
- Anti-fog
- 4 channel PIP
- Image stitching/blending

Video Interfaces
- Sensor input
  - MIPI CSI-2, Parallel 12bits
- Digital input
  - BT.601(8b), BT.656(8b), BT.1120(8/16b)
  - Up to 4 channels
- Digital output
  - BT.601(8b), BT.656(8b), BT.1120(8/16b)
  - LCD Interface (SPI/MCU/RGB Parallel)
  - Up to 2 channels
- Analog output
  - CVBS, HD Analog

Audio Interfaces
- I2S interface for external audio Codec
- Integrated audio codec supporting 8-, 16-, 24-, 32-bit audio inputs and outputs
- Compliance with the G.711 and PCM protocols

On-Chip Interconnect
- Network-on-chip architecture based on AMBA AXI and APB protocol

Neural Processing Unit
- Computation Units
  - 1024 MACs for main computation unit
  - 96 MACs for HW dedicated convolution
- Supported Layers
  - CONV, DW CONV, Activation, Pooling, Upscale
- Support 8-bit integer, Pytorch framework

Peripheral Interfaces
- Universal Peripherals (GPIO 72 mux)
  - Timer/PWM 39ch
  - UART 9ch
  - I2C Master/Slave 9ch
  - SPI Master 9ch
  - Ethernet 10/100/1000 MAC Controller (MII/RMII/RGMII)
  - USB2.0 ULPI Controller
  - I2S Master/Slave 1ch
  - IR Receiver 1ch (NEC)
- SDIO2.0 2ch for Wi-Fi and SD Card
- On-chip ADC (4ch mux type)

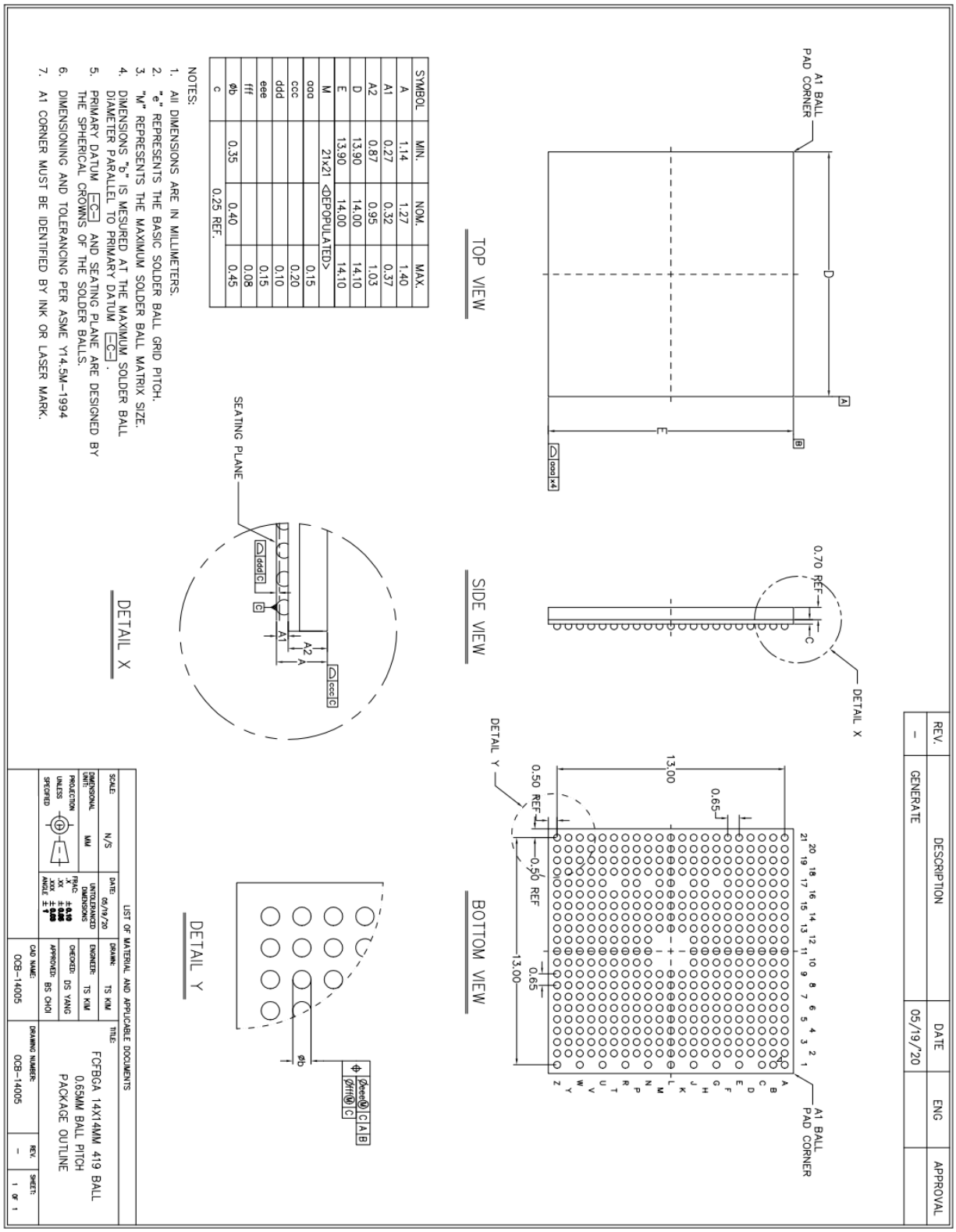
Security Accelerator
- SHA-224/256
- AES-128/256 with ECB/CBC mode
- Checksum 16bit

Memory Interface
- DDR-SDRAM Interface
  - DDR3/DDR3L/LPDDR3 with 32-bit data bus
  - Maximum capacity: 8Gb
- SPI NOR Flash Interface
  - 3-/4-byte address, 1-, 2-, 4-line mode
  - Maximum capacity: 256Mb
- SPI NAND Flash Interface
  - 1-, 2-, 4-line mode
  - Maximum capacity: 2Gb

System Control
- Clock and Reset
- I/O Controller
- DMA 16ch

Physical Specifications
- Operating Voltages
  - 1.8V/3.3V I/O
  - 1.0V Core Power
  - 1.2V/1.35V/1.5V DDR-SDRAM Memory Power
- Package
  - 419 ball FBGA 14mm x 14mm

4. Package Dimension



SYMBOL	MIN.	NOM.	MAX.
A	1.14	1.27	1.40
A1	0.27	0.32	0.37
A2	0.87	0.95	1.03
D	13.90	14.00	14.10
E	13.90	14.00	14.10
M	21x21 <DEPOPULATED>		
aaa			0.15
ccc			0.20
ddd			0.10
eee			0.15
fff			0.08
øb	0.35	0.40	0.45
c	0.25 REF.		

NOTES:
1. All dimensions are in millimeters.
2. "e" represents the basic solder ball grid pitch.
3. "M" represents the maximum solder ball matrix size.
4. Dimensions "b" is mesured at the maximum solder ball diameter parallel to primary datum C.
5. Primary datum C and seating plane are designed by the spherical crowns of the solder balls.
6. Dimensioning and toleranging per ASME Y14.5M-1994
7. A1 corner must be identified by ink or laser mark.

REV.	DESCRIPTION	DATE	ENG	APPROVAL
–	GENERATE	05/19/'20		

< EN675 - 14x14mm, 0.65pitch 419FBGA >

Document Revision History

Version	Date	Description	Modified by
0.1	June. 4, 2020	Initial draft	WH Lee
0.1.1	Sep. 29, 2020	The feature of processor and memory interface has been modified	CL Li
0.2	Oct. 19, 2020	The document has been uploaded and merged into the latest SDK	CL Li
0.2.1	Nov. 11, 2020	The Color type of block diagram has been changed	CL Li
0.2.2	Nov. 30, 2020	Separating the "Peripheral" category	HJ Lee
0.3	Mar. 23, 2021	Modified to engineering sample (Before verification)	HJ Lee
0.3.1	Mar. 24, 2021	Separating the "Accelerator" category	CL Li
1.0	Apr. 13, 2021	Block diagram has been modified.	HJ Lee